IN THE SPECIFICATION:

Please amend the specification as follows:

Pursuant to 37 CFR § 1.121(b)(1)(iii), a marked up copy of each paragraph amended below appears on the page immediately following each amendment.

Please delete page 1, line 1 to page 1, line 8, and insert the following therefor:

-- BACKGROUND

This disclosure relates to a computer system, and more particularly to a mobile computer system using a power conserving processor interfaced with a logic device that allows chipset controllers to pass control signals placing the processor into a deep sleep state or having the logic device [to] place the processor into a deep sleep state in order for the processor to switch power operating modes. --

Please delete page 2, line 10 to page 2, line 21, and insert the following therefor:

-- For mobile PCs, battery power consumption continues to be a major consideration, if not a problem. To conserve battery life, schemes have been implemented to reduce processor operating frequencies and lower voltage. One particular implementation is the Intel® Speedstep™ technology that reduces the operating clock speed of the mobile PC processor and lowers voltage. A frequency and voltage pair is associated with the operating mode. Lower frequency and voltage is referred to as "battery optimized mode." Higher frequency and higher voltage is referred to as "high performance mode." The voltage provided to the processor must meet the core voltage specification for the present operating mode. If an operating mode transition is made, then the system must direct the voltage

processor does not allow assertion of STPCLK* before or soon after reset de-assertion.

All the embodiments with the exception of the simulated S3 and processor only S3 are methods to assure the transition occurs prior to chipset initialization and that the transition to a lower power state other than Quick Start/Stop Grant does not occur prior to the processor being ready for it. The processor being ready is indicated by the Stop Grant Acknowledge bus cycle which we are assuming that the PLD logic will not see because this would require significant additional logic and cost. Sufficient wait is made to assure the processor is reset. --

Please delete page 12, line 1 to page 12, line 6, and insert the following therefor:

-- The output of latch 210 inputted through logical AND gate 305 sets the signal HCYCLE, either halting or continuing a cycle. Other determinative conditions passed through logical AND gate 305 that affect HCYCLE are DISABLE signal and fake suspend to random access memory (RAM) cycle indicator Fake-S3. An output high (value of one) from logical AND gate 305 indicates that a special cycle will be run. An output low (value of zero) from logical AND gate 305 indicates no special cycles. --

Please delete page 14, line 3 to page 14, line 6, and insert the following therefor:

-- Latch 215, latch 220, and latch 225 may be reset when the ENDCYC- signal or the signal SUSRST- are activated low. A compliment of the value of latch 225, the signal STPCLK-, and the signal I_STPCLK- are input into logical AND gate 270 to arrive at the signal C_STPCLK-. --

regulator to regulate to the voltage specification of the other mode. The user, regardless of mode, may also selectively set the operating mode. --

Please delete page 3, line 5 to page 3, line 12, and insert the following therefor:

-- Because communication and control functions are handled by chipset controllers, placing a processor, such as one with Intel® Speedstep™ technology , into C3 or deep sleep requires that chipset controllers have the ability to provide C3 or deep sleep command and control to the processor. Many chipsets, namely desktop PC chipsets, do not have the ability to support such a power state transition and therefore cannot support a processor using Intel® Speedstep™ or similar power conserving technology. The situation is not limited to desktop PC chipsets, but applies to all chipsets that cannot support a C3 power state transition. --

Please delete page 6, line 19 to page 6, line 30, and insert the following therefor:

-- A problem arises as well when a controller, namely a south-bridge controller, has a power management controller that contains logic to detect the Stop Grant Acknowledge bus cycle. The logic and detection are used as an indication that the processor has achieved the Stop Grant state or the Quick Start state. Receipt or detection of the Stop Grant Acknowledge bus cycle is used to trigger transition to the next power state on the processor. After the controller core logic is configured it is possible that one or both of the controllers may respond poorly to an unexpected Stop Grant Acknowledge bus cycle. The processor will send a Stop Grant Acknowledge bus cycle out during the C0 to C3 transition needed to force the transition of the processor to performance mode. Because something other than the north-bridge controller or the south-bridge controller caused the transition, the resulting Stop Grant Acknowledge bus cycle is not expected to occur. --

Please delete page 7, line 1 to page 7, line 18, and insert the following therefor:

-- Without support of power state transitions it is very unlikely that neither the south-bridge controller nor the north-bridge controller would do anything other than pass the Stop Grant Acknowledge bus cycles when they occur. Prior to chipset initialization it is most likely that the chipset will merely pass through cycles it has not been configured to accept or respond to.

Chipsets and chipset controllers that are not designed to work with power saving processors such as an Intel® Speedstep™ processor are unable to pass power state transition signals through because the controllers lack the necessary control and logic. The processor therefore cannot be placed into a C3 state in order to change system operating mode.

SUMMARY

Problems identified above are addressed by the present disclosure of transitioning power states of processors using separate logic control. This disclosure relates to providing logic that will enable a chipset to transition a power conserving processor into "deep sleep" or C3 state, and also to transition the processor to "operating" or C0 state. This disclosure allows previously non-compatible chipsets to work with power conserving processors, processors frequently used in a mobile PC system. --

Please delete page 8, line 14 to page 8, line 23, and insert the following therefor:

-- One embodiment includes where the logic looks for the first fetch to ROM to trigger the assertion of the STPCLK* signal. This would be useful in cases where a

Please delete page 14, line 20 to page 14, line 27, and insert the following therefor:

-- S3 is an ACPI defined system state and generally refers to a suspend to random access memory (RAM) condition. In the S3 state power is turned off to everything except system memory, the memory controller, and the power management controller (power management control logic). S0 is an operating system state. By allowing a system to perform an S3 state transition, the capability exists to have the processor perform a power state transition. As the system enters S3 state, the processor enters into C3 state and when exiting C3 is able to make the performance mode changes. --

Please delete page 15, line 25 to page 15, line 32, and insert the following therefor:

-- The BIOS initiates an S3 state transition on the chipset. The chipset transitions the system into S3 state except that the PLD blocks the reset to the system and the processor and also prevents the power supplies from being turned off. The PLD transitions the processor to the C3 state instead of the off state. The chipset however does see a reset.

As soon as the chipset gets the system into the S3 state the PLD assets a "wake" condition (O-WAKE- goes low) causing the chipset to immediately begin an S3 to S0 state transition. --

Please delete page 16, line 7 to page 16, line 19, and insert the following therefor:

-- The value FAKE_S3 and the disable signal DISABLE –(active when the value is set low) are input into logical AND gate 280, the output of logical AND gate 280 is the signal FKE_S3. FKE_S3 and the compliment value of I_SLP_S3- (signal

indicating that system is in S3 mode) are input into logical AND gate 285. The output of AND gate 285 enables latch 235. Latch 235 receives the clock pulse signal SUSCLK, and outputs a high value (value of one) on the first rising edge of SUSCLK when enable is high.

The complement value of the output of latch 235 is defined as the signal O_WAKE, which is the wake signal to the power management controller. The FKE_S3 signal and the I_SLP_S3- signal are input into logical OR gate 287. The output of logical OR gate 287 and the SUSRST- signal re input into logical AND gate 290. The output of logical AND gate 290 is O_SLP_S3 is the output SLEEP_S3 signal to the system electronics. --

Please delete page 16, line 30 to page 17, line 6, and insert the following therefor:

-- Performance mode setting is represented by the signal P_LO/HI-. P_LO/HI- is an input value received by the PLD. The compliment value of P_LO/HI- and the signal DISABLE- signal are input into logical AND gate 292, the value of output of AND gate 292 is stored in latch 245. Latch 245 outputs the value as the signal GMUXSEL. The compliment value of Latch 245 is a PLD output value called CPUPERF. A low value (value of zero) for CPUPERF- represents the high performance mode, and a high value (value of one) represents the battery optimized mode. The VRMPWRGD signal is the signal to the PLD showing that core regulator power is good. VRMPWRGD, the value of latch 215, and FKE_S3 are input into logical OR gate 295, and the output value of OR gate 295 is GDRUNPWROK. --

Please delete page 17, line 29 to page 18, line 5, and insert the following therefor:

-- The north-bridge controller 106 interfaces to the processor 102 via a processor bus, however, other communication busses may be used. The north-

bridge controller 106 interfaces to a south-bridge controller 104 via a PCI bus; however, other communications busses may be used. The north-bridge controller 106 interfaces to a south-bridge controller 104 via a PCI bus; however, other communications busses may be used. In this particular disclosure, the PCI reset signals are shown which relate to the power state transitions to be made to the north-bridge controller 106. The PLD 100 sends a signal O_PCIRST- to the north-bridge controller 106. North-bridge controller 106 receives this as a PCIRST- signal. The PCIRST- signal is the PCI reset signal. The north-bridge controller 106 in turn sends out a CPURST- signal back to the PLD 100. The CPURST- signal is the processor reset signal input to the PLD 100. --

Please delete page 20, line 3 to page 20, line 7, and insert the following therefor:

-- ICH2M 114 output signals SLP_S3- and SUSSTAT- go to the PLD 100 and are passed through on PLD 100 output signals SLP_S3- and SUSSTAT-. These signals are passed through the PLD 100 unless a Fake S3 cycle is run. These signals typically control power planes within a portable computer and are controlled by the PLD 100 for Fake_S3 cycles. --

Please delete page 20, line 20 to page 20, line 33, and insert the following therefor:

-- The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the disclosure. However, it will be apparent to one skilled in the art that specific details are not required in order to practice the embodiments. Thus, the foregoing descriptions of specific embodiments of the present disclosure are presented for purposes of illustration and description; they are not intended to be exhaustive or to limit the disclosure to the precise forms disclosed, obviously many modifications and variations are possible in view of the above teachings. For example, different logic may be employed using

similar discrete components. Different timing diagrams may be employed to transition power states. The embodiments were chosen and described in order to best explain the principles of the disclosure and its practical applications and to thereby enable others skilled in the art to best utilize the various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the disclosure be defined by the following claims and their equivalents: --

A13 end